151. (Amended) A method of controlling a memory device by a memory controller, wherein the memory device includes a plurality of memory cells, the method of controlling the memory device comprises:

providing first block size information to the memory device, wherein the first block size information is provided by the memory controller and is representative of a first amount of data to be input by the memory device; and

issuing a first operation code to the memory device, wherein in response to the first operation code, the memory device inputs the first amount of data.

152. The method of claim 151 wherein the memory device inputs the first amount of data synchronously with respect to an external clock signal.

153. (Amended) The method of claim 151 further including:

providing second block size information to the memory device, wherein the second block size information defines a second amount of data to be input by the memory device; and

issuing a second operation code to the memory device, wherein in response to the second operation code, the memory device inputs the second amount of data.

154. (Amended) The method of claim 151 wherein the first block size information and the first operation code are included in a request packet.

155. (Amended) The method of claim 154 wherein the first block size information and the first operation code are included in the same request packet.

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6 ~~156~~. (Amended) The method of claim 1 ~~151~~ further including providing the first amount of data to the memory device.

7 ~~157~~. (Amended) The method of claim 6 ~~156~~ wherein the first amount of data is provided to the memory device after a delay time transpires.

8 ~~158~~. (Amended) The method of claim 7 ~~157~~ wherein the delay time is representative of a number of clock cycles of an external clock signal.

9 ~~159~~. (Amended) The method of claim 1 ~~151~~ wherein the first block size information is a binary representation of the first amount of data.

10 ~~160~~. (Amended) The method of claim 1 ~~151~~ wherein the first amount of data is output, by the memory controller, synchronously with respect to an external clock signal and during a plurality of clock cycles of the external clock signal.

14 ~~161~~. (Amended) A method of operation in a synchronous memory device, wherein the memory device includes a plurality of memory cells, the method of operation of the memory device comprises:

receiving first block size information from a memory controller, wherein the first block size information represents a first amount of data to be input by the memory device in response to an operation code;

receiving the operation code, from the memory controller, synchronously with respect to an external clock signal; and

inputting the first amount of data in response to the operation code.

15 ~~162~~. (Amended) The method of claim 14 ~~161~~ wherein inputting the first amount of data includes receiving the first amount of data synchronously with respect to the external clock signal.

163. (Amended) The method of claim 162 wherein the first amount of data is sampled over a plurality of clock cycles of the external clock signal.

164. (Amended) The method of claim 161 wherein the first block size information and the operation code are included in a request packet.

165. (Amended) The method of claim 164 wherein the first block size information and the operation code are included in the same request packet.

166. (Amended) The method of claim 161 wherein the first block size information is a binary representation of the first amount of data to be input in response to the operation code.

167. (Amended) The method of claim 161 wherein the first amount of data is output, by the memory controller, synchronously during a plurality of clock cycles of the external clock signal.

168. (Amended) The method of claim 161 further including generating an internal clock signal, using a delay locked loop and the external clock signal wherein the first amount of data is input synchronously with respect to the internal clock signal.

169. (Amended) The method of claim 161 further including generating first and second internal clock signals using clock generation circuitry and the external clock signal, wherein the first amount of data is input synchronously with respect to the first and second internal clock signals.

23 ~~170~~. The method of claim 22 ~~169~~ wherein the first and second internal clock signals are generated by a delay lock loop.

29 ~~171~~. (Amended) A method of operation of an integrated circuit, wherein the integrated circuit includes a dynamic random access memory array having a plurality of memory cells, the method of operation comprises:

Am 73 > receiving block size information from a controller, wherein the block size information represents an amount of data to be input in response to an operation code; 1st 73

receiving the operation code from the controller; and

inputting the amount of data in response to the operation code.

Cancel E1

30 ~~172~~. (Amended) The method of claim 29 ~~171~~ further including storing the amount of data in the memory array.

31 ~~173~~. (Amended) The method of claim 29 ~~171~~ wherein the block size information and the operation code are included in a request packet.

32 ~~174~~. (Amended) The method of claim 29 ~~171~~ wherein the block size information is a binary representation of the amount of data to be input in response to the operation code.

33 ~~176~~. (Amended) The method of claim 29 ~~171~~ wherein the amount of data is input, in response to the operation code, after a delay time transpires.

34 ~~177~~. The method of claim 33 ~~176~~ wherein the delay time is representative of a number of clock cycles of the external clock signal.

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Kindly **ADD** the following claims:

16 1
178. (New) The method of claim 151 wherein the first operation code is issued onto a bus.

17 11
179. (New) The method of claim 178 wherein the bus includes a plurality of signal lines to multiplex control information, address information and data.

18 1
180. (New) The method of claim 151 further including providing address information to the memory device.

24 14
181. (New) The method of claim 161 wherein the operation code, the first block size information and address information are included in a packet.

25 14
182. (New) The method of claim 161 further including receiving address information from the memory controller.

26 14
183. (New) The method of claim 161 wherein the first block size information, and the operation code are received from an external bus.

27 26
184. (New) The method of claim 183 wherein the first block size information, and the operation code are received from the same external bus.

28 27
185. (New) The method of claim 184 wherein the external bus is used to multiplex address information, control information and data.

35 29
186. (New) The method of claim 171 further including receiving address information from the controller.